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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,741	08/01/2001	Michael Tate	41257/PAN/X2/134038	8731
35114	7590	10/19/2004	EXAMINER	
ALCATEL INTERNETWORKING, INC. ALCATEL-INTELLECTUAL PROPERTY DEPARTMENT 3400 W. PLANO PARKWAY, MS LEGL2 PLANO, TX 75075			CHEN, ALAN S	
			ART UNIT	PAPER NUMBER
			2182	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center">Office Action Summary</p>	<p>Application No.</p> <p align="center">09/921,741</p>	<p>Applicant(s)</p> <p align="center">TATE, MICHAEL</p>	
	<p>Examiner</p> <p align="center">Alan S Chen</p>	<p>Art Unit</p> <p align="center">2182</p>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.


- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06/14/2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 and 46-50 is/are pending in the application.
- 4a) Of the above claim(s) 29-45 is/are withdrawn from consideration.
- 5) ☐ Claim(s) 17-28 is/are allowed.
- 6) ☒ Claim(s) 1-16 and 46-50 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.


FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____</p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6) <input type="checkbox"/> Other: _____</p> |
|--|---|

DETAILED FINAL ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 8-10, 13, 46-48 and 50 are rejected under 35 USC 103(a) as being unpatentable over 5,950,223 to Chiang et al. (hereafter Chiang) in view of No. 6,590,901 to Jones.

3. As per claim 1, Chiang discloses a method for maintaining throughput in a data element (Fig. 3, maintaining throughput at both clock edges, the data element being a DRAM), comprising the steps of: receiving a clock (Fig. 5A and 5B CAS clock lines) and a plurality of instances of data having a first width (Fig. 7A, element DQ) on an input; processing (e.g., latching 32-bit data, Column 3, lines 52-58) consecutive ones of the plurality of instances of data having the first width (32-bit data latched, and upon the next clock edge, producing another 32-bit data to be latched) to produce more than one of a plurality of instances of data having a second width wherein the second data width are equivalent to the first data width (Fig. 7A, DO1, DO2 and DOn are all the same width, and the first width is picked up on the rising edge of CAS, while the second width is picked up on the falling edge of the clock, hence dual data/edge rate sampling of data) and the more than one of the plurality of instances of data having the second data width are used to produce a plurality of instances of data having a third data width (Column 3, lines 52-58, 64-bit data produced with both first and second width data) wherein the third data width are greater than the second data width the plurality of instances of data having a third data

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width are used to produce a plurality of instances of data having an output data width (output of 64-bit data may be placed into an I/O buffer for instance, Fig. 3, element 334) wherein the output data width are equivalent to the third data width (I/O buffer is same 64-bit width as the 64-bit latch that was produced from two 32-bit words); and transmitting the plurality of instances of data having the output data width and transmitting the plurality of instances of data having the third data width (transmission out of memory device Fig. 3 via a read operation).

Chiang does not disclose expressly the clock and plurality of instances of data being received in a switch, e.g., the memory disclosed by Chiang being used inside a switch that comprises at least one media access controller.

Jones discloses RAM being used in a network switch (Fig. 6 and Column 3, lines 15-20). Jones also discloses the desire to increase the speed of DRAM in the network switch (e.g., Column 5, lines 50-Column 6, lines 13)

Chiang and Jones are analogous art because they are from similar problem solving area in reducing latency in DRAM to improve performance of the overall system that the memory is embedded/attached to.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Chiang's invention to dramatically increase the speed of the DRAM in Jones and thereby improving the overall network switch performance (Fig. 6 and 7).

The suggestion/motivation for doing so would have been that Chiang provides a dramatic improvement for DRAMs by, *inter alia*, using both edges of the clock, and DRAM is used in a wide variety of applications, in particular, network switches such as Jones where improvements from Chiang would significantly boost performance. It should be emphasized that Chiang is an

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improvement of DRAM which is not a standalone computer product, but is incorporated and operational with other computer components in a vast amount of different computer product applications that require memory. Jones is an example where the DRAM is incorporated into a network switch.

Therefore, it would have been obvious to combine Chiang with Jones for the benefit of using the latest/faster DRAM to improve overall system performance in a network switch.

4. As per claim 8-10, Chiang combined with Jones discloses the method of claim 1, Chiang further disclosing the processing step includes sampling the data at dual clock edges at the rising and falling edge of a clock (Fig. 7A) each sample being 32 bits (first and second width) and the producing a 64 bit word (third and fourth width (Column 3, lines 50-58)).

5. As per claim 13, Chiang combined with Jones discloses the method of claim 1, Chiang further disclosing the step of resolving a data alignment (the use of 64 bit data is aligned using two 32 bit data obtained from consecutive rising and falling clock edges, Fig. 7A).

6. As per claim 46, Chiang discloses a method for maintaining throughput in a data element (Fig. 3), comprising the steps of: receiving a first data having first bit-width bits (Fig. 3, element 334), management bits and clock bits (Fig. 3, signals lines OE, WE, CASH, CASL, etc);

inputting the first bit-width bits and clock bits into a receive path (receive data paths show as lines to modules); and processing the first bit-width bits to generate processed data having a

~~second bit-width which is greater than said first bit-width (Column 3, line 50-58, where 32 bits is~~

the first width while 64 bits is the second width). Note that the memory of Chiang is hardware and by definition belongs to the physical layer. The examiner takes official notice that hardware

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is defined as being the physical layer one of the seven layer OSI model. A MAC device belongs to the network layer.

Chiang does not disclose expressly the first data, management bits and clock bits received in a switch, e.g., the memory disclosed by Chiang being used inside a switch.

Jones discloses RAM being used in a network switch (Fig. 6 and Column 3, lines 15-20). Jones also discloses the desire to increase the speed of DRAM in the network switch (e.g., Column 5, lines 50-Column 6, lines 13).

Chiang and Jones are analogous art because they are from similar problem solving area in reducing latency in DRAM to improve performance of the overall system that the memory is embedded/attached to.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Chiang's invention to dramatically increase the speed of the DRAM in Jones and thereby improving the overall network switch performance (Fig. 6 and 7).

The suggestion/motivation for doing so would have been that Chiang provides a dramatic improvement for DRAMs by, *inter alia*, using both edges of the clock, and DRAM is used in a wide variety of applications, in particular, network switches such as Jones where improvements from Chiang would significantly boost performance. It should be emphasized that Chiang is an improvement of DRAM which is not a standalone computer product, but is incorporated and operational with other computer components in a vast amount of different computer product applications that require memory. Jones is an example where the DRAM is incorporated into a network switch.

Therefore, it would have been obvious to combine Chiang with Jones for the benefit of using the latest/faster DRAM to improve overall system performance in a network switch.

7. As per claims 47 and 48, Chiang combined with Jones discloses the method of claim 46, wherein the processing step further comprises: receiving a clock having a clock rate (Fig. 7A, CAS line has periodicity which equals a rate); and performing dual data rate sampling (rising and falling edge sampling of the clock, Fig. 7A) on the first bit width data in accordance with said clock to produce the processed data having a second bit-width which is greater than the first bit-width (Column 3, lines 50-58, where 32 bits is first width, 64 bits is second width).

8. As per claim 50, Chiang combined with Jones discloses the method of claim 47, wherein the step of performing dual data rate sampling on the first bit-width bits comprises inputting the first bit-width bits to two gates (Fig. 5A strobe signals 1 and 2 are gates that latch data at rising and falling edge of clock CAS), one gate triggering at a rising edge of the clock (Fig. 5A, 1st data strobe) and the other gate triggering on a falling edge of the clock (Fig. 5A, 2nd data strobe).

9. Claims 2-4, 15 and 16 are rejected under 35 USC 103(a) as being unpatentable over Chiang in view of Jones in further view of PCI Local Bus Specification Rev. 2.1 (hereafter PCI Spec).

10. As per claim 2-4 and 15 Chiang combined with Jones discloses the method according to claim 1, the processing step further comprising the steps of sampling consecutive ones of the plurality of instances (Fig. 7A) having the first width at consecutive ones of a first rising edge and falling edge of the clock (DO1 and DO2 of 7A can be the first width); generating more than one instance of a plurality of data having the second width (the second width is the same as the

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first width); Chiang further discloses generating and transmitting a third width that is double the first and second width (Column 3, lines 50-58).

Chiang combined with Jones does not expressly disclose converting the more than one instance of the plurality of data having the second width at a second rising edge of the clock to result in the plurality of instances of data having the third width data or transmitting a handshake signal; and transmitting the plurality of instances of data having the third data width.

PCI Spec discloses ability for the PCI bus to handle 64 bit data and addressing. PCI Spec details what is needed in latching in an additional 32 bits of data and the handshaking required (e.g., ACK64 and REQ64, page 16 of PCI Spec which are pulses, specifically sustained pulses, page 8, s/t/s). Furthermore, PCI Spec uses the rising edge of the clock, and hence, the second 32-bit piece of data is latched in on the second rising edge after the first one is latched in.

Chiang combine with Jones and PCI Spec are analogous art because they are from the same field of endeavor in how to increase throughput on a data bus.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use handshaking and latch data on the second rising edge of the clock.

The suggestion/motivation for doing so would have been the need to request/acknowledge a double word bit transfer in a bussing/addressing system that transfers only one word per clock edge. Furthermore, this follows an omnipresent bus specification used and well known to the entire computer industry.

Therefore, it would have been obvious to combine Chiang and Jones with PCI Spec for the benefit of transferring a double word on single word bus architecture and abiding by a well-established specification.

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11. As per claim 16, Chiang and Jones combined with PCI Spec discloses the method according to claim 15, wherein Chiang further specifies the use of I/O buffers (encompassing FIFOs) to be used in I/O transactions (Fig. 3, element 334), where handshaking could occur.

12. Claim 5 is rejected under 35 USC 103(a) as being unpatentable over Chiang in view of Jones in further view of PCI Spec.

Chiang and Jones combined with PCI Spec discloses claim 2.

Chiang and Jones combined with PCI Spec do not disclose expressly the clock being received from a media independent interface.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to receive the clock from a media independent interface.

The suggestion/motivation for doing so would have been the generic memory implementation described by Chiang can be used wherever there requires a storage location, and a media independent interface is no exception. Further PCI Spec is also a generic specification. Both show the clock coming in from an external source.

Therefore, it would have been obvious receive the clock from an external source such as a media independent interface for the benefit of the generic memory receiving a clock signal from the outside since it is not generated internally.

13. Claim 49 is rejected under 35 USC 103(a) as being unpatentable over Chiang in view of Jones.

Chiang combined with Jones discloses claim 47.

Chiang combined with Jones do not disclose expressly the clock being received from a media independent interface.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to receive the clock from a media independent interface.

The suggestion/motivation for doing so would have been the generic memory implementation described by Chiang can be used wherever there requires a storage location, and a media independent interface is no exception.

Therefore, it would have been obvious receive the clock from an external source such as a media independent interface for the benefit of the generic memory receiving a clock signal from the outside since it is not generated internally.

14. Claims 6, 7, 11, 12 and 14 are rejected under 35 USC 103(a) as being unpatentable over Chiang in view of Jones in further view of No. US005812792A to Haddock et al. (hereafter Haddock).

Chiang combined with Jones discloses claim 1.

Chiang combined with Jones does not disclose expressly his generic DRAM implementation used in a network system, and therefore not having CRC, statistics generation, resolving inter-packet gap, resolving preamble detection, resolving statistics or a management control element.

Haddock discloses using DRAM in a network system, having CRC (Column 8, lines 48-67), statistics generation (Column 16, lines 40-65), resolving inter-packet gap (timing differences resolution, Column 16, lines 32-39), resolving preamble detection (Fig. 11, preamble in frame), resolving statistics (Column 16, lines 40-65), having a physical layer device (Fig. 2), or a management control element (Fig. 5).

Chiang combined with Jones and Haddock are analogous art because they are from the same field of endeavor in the use and implementation of DRAM.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chiang combined with Jones DRAM in a network system.

The suggestion/motivation for doing so would have been to be able to accommodate multiple clients who have multiple displays requiring video DRAM) on a network (Fig. 1), and hence requiring fast memory access that Chiang combined with Jones provides with sampling on the rising and falling edges of the clock.

Therefore, it would have been obvious to combine Chiang, Jones and Haddock for the benefit of fast video DRAM in a network environment.

Response to Arguments

15. Applicant's arguments with respect to claims 1,8-10,13, 46-48 and 50 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

16. Claims 17-28 are allowed.

17. The following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, a method for maintaining throughput in a data element and relating the first, second, third, fourth elements, as stated, having certain bit widths to specific components of a media access controller.

Conclusion

18. The prior art made of record is considered pertinent to applicant's disclosure as proof of the physical layer, which Examiner has taken official notice on.

The 7 layers of the OSI Model from www.webopedia.com

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
09/30/2004


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